

**REMARKS****Claim Rejections 35 U.S.C. § 103 (a)**

The Examiner has rejected claims 1-11 under 35 U.S.C. §103 (a) as being unpatentable over Satya et al. (US 6,528,818) in view of Gallarda et al. (US 6,539,106).

Applicants respectfully disagree with the Examiner. Applicants have amended claim 1. Claim 1, as amended, of Applicants' claimed invention, claims a structure (250) that includes a first set (245) of features located in a scribeline, the first set of features being a subset of product features; and a second set (255) of features located in the scribeline and merged directly into the first set of features, the second set occupying a smaller area than the first set, the second set being similar to the first set, the second set being distinguishable from surrounding structures by pattern recognition and evaluation of contrast, density, tone, and grey scale in an image. Support is provided at lines 5-22 on page 8 of the specification.

In contrast, the Satya et al. reference cited by the Examiner teaches a die array (202), as shown in figure 4A, that includes test dies (204) and product dies (206) separated by scribelines, as shown in Figure 4B, where test structures are located within the test die (204). See Figure 4B. Also, see Col. 11, lines 38-44. Thus, the test structure of Satya et al. is not located in a scribeline, as claimed in claim 1, as amended, of Applicants' claimed invention.

The Examiner states that Satya et al. further teaches that each test die (204) is configured to have a number of portions, namely, a first portion (206) and a second portion (208) separated by an intermediate portion (210). See Figure 4C. Also, see Col. 11, lines 38-44.

However, the Examiner concedes that Satya et al. does not specifically mention or describe the second set of features occupying a smaller area than the first set. See lines 12-13 on page 3 of the Office Action mailed January 6, 2005.

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In the opinion of the Examiner, Gallarda et al. describes the second set (536) of features occupying a smaller area than the first set (526, 528, 530, 532, 534). See Figure 5. See lines 14-16 on page 3 of the Office Action mailed January 6, 2005.

Applicants submit that the Examiner has mischaracterized Gallarda et al. The cited Gallarda et al. reference clearly teaches a split-screen view of a reference image (410) taken of a first die, shown on the left side, juxtaposed next to a test image (420) taken of a second die, shown on the right side. See Figure 4. Also, see Col. 6, lines 41-43. Thus, the structure of Gallarda et al. is also not located in a scribeline, as claimed in claim 1, as amended, of Applicants' claimed invention.

Gallarda et al. further teaches that since the reference image (410) and the test image (420) occupy areas having the same size, they may be aligned to match features from the two images, thus identifying those features that have no counterparts. In particular, Gallarda et al. clearly describes the first set, or reference image (510), as including five features (512, 514, 516, 518, 520) and the second set, or test image (524), as including six features (526, 528, 530, 532, 534, 536), where the features from the two images are contact holes having the same pitch and the same critical dimension. See Figure 5. Also, see Col. 6, lines 54-58.

Thus, a combination of the structures of Satya et al. and Gallarda et al. would still not produce the merged scribeline structure claimed by Applicants in claim 1, as amended, of Applicants' claimed invention.

Consequently, the two references cited by the Examiner do not, individually or collectively, teach, suggest, or render obvious the structure of Applicants' claimed invention, as claimed in claim 1, as amended, to one of ordinary skill in the art of fabricating semiconductors at the time that the invention was made.

Claims 2-11 are dependent on claim 1, as amended. As discussed previously, Applicants' claimed invention, as claimed in claim 1, as amended, would not have been obvious to one of ordinary skill in the art of fabricating semiconductors at the time that the invention was made. Thus, Applicants' claimed invention, as claimed in claims 2-11, would also not have been obvious to one of ordinary skill in the art of semiconductors at the time that the invention was made.

In view of the foregoing, Applicants respectfully request the Examiner to withdraw the rejections to claims 1-11 under 35 U.S.C. §103 (a).

Applicants believe that all claims pending, including amended claim 1, are now in condition for allowance so such action is earnestly solicited at the earliest possible date.


Pursuant to 37 C.F.R. 1.136(a)(3), Applicants hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time.

Should there be any additional charges, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, please charge Deposit Account No. 02-2666.

If a telephone interview would in any way expedite the prosecution of this application, the Examiner is respectfully invited to contact the undersigned at (408) 720-8300.

Respectfully submitted,  
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